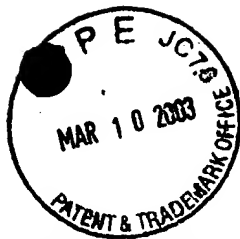


Docket No.: 57454-138



#14/D

PATENT

3/17/03

Adm H

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Yasuhiko TSUKIKAWA

Serial No.: 09/877,027

Group Art Unit: 2816

Filed: June 11, 2001

Examiner: Linh M. NGUYEN

For: CONFIGURATION FOR GENERATING A CLOCK INCLUDING A DELAY CIRCUIT
AND METHOD THEREOF

SUPPLEMENTAL AMENDMENT

Assistant Commissioner for Patents
Washington, DC 20231

RECEIVED
MAR 11 2003
TECHNOLOGY CENTER 2800

Sir:

The following amendment and remarks are supplemental to the response filed on January 21, 2003. Please amend the application as follows.

IN THE CLAIMS

Please amend claims 4 and 11 as follows:

4. (Three Times Amended) A semiconductor device comprising a delay locked loop including:
- an input buffer receiving an external clock and outputting a first internal clock;
 - a delay circuit delaying said first internal clock to output a second internal clock;
 - a detector detecting which of said first and second clocks is advanced in a phase; and

E17

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